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08/922,300	09/02/97	PARK G	P54766

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EXAMINER	
MARC COLEMAN,M	
ART UNIT	**PAPER NUMBER**
3661	15

DATE MAILED: 11/13/00

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

U.S. G.P.O. 2000 ; 465-168/25268

Office Action Summary	Application No.	Applicant(s)	
	08/922,300	PARK, GEUN-WOO	
	Examiner	Art Unit	
	Marthe Y. Marc-Coleman	3661	

-- The MAILING DATE of this communication app ars on the cover she t with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *three* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 September 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 September 1997* is/are objected to by the Examiner.

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. & 119(e).

Attachment(s)

15) ☒ Notice of References Cited (PTO-892)
16) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
17) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
18) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
19) ☐ Notice of Informal Patent Application (PTO-152)
20) ☐ Other: .

DETAILED ACTION

1. This office action is responsive to applicant's appeal brief filed on 9/25/00. Based upon argument presented on the appeal brief, a new ground of rejection is established. **The final office action is withdrawn and Examiner reopens prosecution.**

Drawings

2. The drawing is objected to because Fig. 2 should label prior art. Appropriate correction is required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant admitted prior art in view of Van Clifton Martin (U.S. Patent No. 3,555,348).

In regard to claims 1 and 4, Applicant discloses in the background of the invention:

- a pulse width modulation (PWM) controller for generating a PWM signal under the control of the microcomputer;

- a current amplifier for amplifying current in response to the PWM signal from the PWM controller;

-a horizontal/vertical (H/V) processor for driving a horizontal driver under the control of a microcomputer;

- the H/V processor outputs a horizontal pulse signal of square wave to the horizontal driver under the control of a microcomputer;

- a horizontal deflection coil is mounted to the neck of a display device so that electron beams can be deflected to the left or right according to a direction of current flowing through the coil;

- an S-correction capacitor applies a parabola voltage to the horizontal deflection coil to correct a linearity of center-to-left and right sides of a screen of the display device;

- a horizontal output circuit for supplying current to a horizontal deflection coil and an S-correction capacitor in response to output signals from the current amplifier and horizontal driver;.

- a horizontal/vertical (H/V) processor constant voltage circuit for supplying a constant voltage to the H/V processor to drive it;

Applicant admitted prior art does not disclose a power interruption delay charging means for gradually lowering said input voltage to said H/V processor constant voltage circuit when power supplied to said display device is interrupted.

Van Clifton Martin discloses that the control grid 14 is clamped to a negative DC bias voltage -V1 from the power supply by a diode 44 connected between voltage -V1 and the control grid 14 and a capacitor 45 connected between the control grid 14 and ground. The output of the unblank driver 22 thereby controls the voltage between the control grid 14 and the cathode 13 by controlling the voltage of cathode 13. **This diode-**

capacitor network makes the voltage at the control grid 14 drop slowly even though its bias voltage -V1 is removed (see col. 2 lines 64-72).

At the time of the invention, it would have been obvious to one skilled in the art to utilize Van Clifton Martin's protection circuit with Applicant admitted prior art because it would protect the CRT display in case of sudden failures or malfunctions or circuits to the tube(see Van Clifton Martin col. 1 lines 36-39).

In regard to claim 3, Applicant admitted prior art discloses:

- a power supply circuit is adapted to convert commercial alternating current (AC) into direct current (DC) (see page 2 of the background of the invention lines 1-2).
- a horizontal deflection circuit under the control of a microcomputer, receiving said direct current input voltage, for horizontally deflecting electron beams generated in the cathode ray tube (see page 2 background of the invention lines 5-8).

Applicant admitted prior art does not disclose a power interruption delay charging means for gradually lowering said direct current input. In addition, Applicant's admitted prior art does not disclose a polarity capacitor and a diode connected to said polarity capacitor.

Van Clifton Martin discloses that the control grid 14 is clamped to a negative DC bias voltage -V1 from the power supply by a diode 44 connected between voltage -V1 and the control grid 14 and a capacitor 45 connected between the control grid 14 and ground. The output of the unblank driver 22 thereby controls the voltage between the control grid 14 and the cathode 13 by controlling the voltage of cathode 13. **This diode-capacitor network makes the voltage at the control grid 14 drop slowly even though its bias voltage -V1 is removed** (see col. 2 lines 64-72 and col. 7 lines 10-14).

At the time of the invention, it would have been obvious to one skilled in the art to utilize Van Clifton Martin's protection circuit with Applicant admitted prior art because it would protect the CRT display in case of sudden failures or malfunctions or circuits to the tube(see Van Clifton Martin col. 1 lines 36-39).

In regard to claims 5 and 8, Applicant admitted prior art discloses in Fig.2 and background of the invention:

- a pulse width modulation (PWM) controller for generating a PWM signal under the control of the microcomputer;
- a horizontal deflection coil for horizontally deflecting electron beams generated in said display device;
- a current amplifier transformer having a primary coil and a secondary coil (see T1);
- a field effect transistor having its gate terminal connected to one terminal of said secondary coil (see FET1);
- one terminal of said primary coil being connected to an output terminal of said pulse width modulation controller 135 through a capacitor and another terminal of said primary coil being connected to the ground terminal;
- said field effect transistor having a drain terminal connected to a high voltage source B+ and a source terminal connected in common to a second terminal of said secondary coil and one other side of a pulse transformer PT;
- said pulse transformer having a second side connected to one side of said horizontal deflection coil;".
- a first diode connected between said source terminal and said drain terminal;

- a second diode connected between said second terminal of said secondary coil and said ground terminal;
- a H/V processor for generating a square wave pulse signal under the control of said microcomputer;
- a horizontal driver 144 for generating a drive pulse signal in response to the square wave pulse signal from said H/V processor;
- an S correction capacitor applies a parabola voltage to the horizontal deflection coil to correct a linearity of center-to-left and right sides of a screen of the display device;
- a horizontal output circuit for supplying current to a horizontal deflection coil and an S-correction capacitor in response to output signals from the current amplifier and horizontal driver;.
- a horizontal/vertical (H/V) processor constant voltage circuit for supplying a constant voltage to the H/V processor to drive it;

Applicant admitted prior art does not disclose a power interruption delay charging means for gradually lowering said input voltage to said H/V processor constant voltage circuit when power supplied to said display device is interrupted.

Van Clifton Martin discloses that the control grid 14 is clamped to a negative DC bias voltage -V1 from the power supply by a diode 44 connected between voltage -V1 and the control grid 14 and a capacitor 45 connected between the control grid 14 and ground. The output of the unblank driver 22 thereby controls the voltage between the control grid 14 and the cathode 13 by controlling the voltage of cathode 13. **This diode-capacitor network makes the voltage at the control grid 14 drop slowly even though its bias voltage -V1 is removed** (see col. 2 lines 64-72).

At the time of the invention, it would have been obvious to one skilled in the art to utilize Van Clifton Martin's protection circuit with Applicant admitted prior art because it

would protect the CRT display in case of sudden failures or malfunctions or circuits to the tube(see Van Clifton Martin col. 1 lines 36-39).

In regard to claims 2 and 9, Van Clifton Martin discloses :

- a polarity capacitor for performing charging operation and a diode connected to the polarity capacitor for preventing a voltage on the polarity capacitor from being discharged (see col. 2 lines 64-72 and Fig. 1 element 45).
- a diode connected to said polarity capacitor, for preventing a voltage charged on said polarity capacitor from being discharged to a power supply circuit when the power supply to the display device is interrupted (see col. 2 lines 64-72 and Fig. 1 element 44).

In regard to claims 6 and 10, Applicant's admitted prior art discloses in Fig. 2: said horizontal output circuit 234 comprises a horizontal output transistor TR having a collector terminal connected in common to said second side of said pulse transformer T2 and said one side of said horizontal deflection coil H-DY, an emitter terminal connected to said S-correction Capacitor Cs and said ground terminal, and a base terminal connected to an output terminal of said horizontal driver for receiving said drive pulse signal.

In regard to claims 7 and 11, Applicant's admitted prior art discloses in Fig. 2:

- a second field effect transistor FET2 having a gate terminal connected to receive a square wave pulse signal from said horizontal/vertical processor 132, a source terminal connected to said ground terminal, and a drain terminal;

- a horizontal drive transformer T2 having a primary coil and a secondary coil, said primary coil having one terminal connected to a voltage source V2 through a resistor and a second terminal connected to said drain terminal of said second field effect transistor; and
- said secondary coil of said horizontal drive transformer T2 having one said connected to said base terminal or said horizontal output transistor 134 and a second side connected to said ground terminal.

5. The prior arts made of record and not relied upon are considered pertinent to applicant's disclosure (e.g. Leaver , Arai et al., Jackson et al., Morrish, Hamaguchi et al., Choi, Jung et al., Walker et al., Lendaro, Norman et al.).

Response to Arguments

6. Applicant's arguments filed on 9/25/00 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Marthe Y. Marc-Coleman whose telephone number is (703) 305-4970. The examiner can normally be reached on Monday - Friday (5:30AM - 3:00PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, William Cuchlinski can be reached on (703) 308-3873. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 305-7687 for regular communications and (703) 308-8623 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-1111.

WILLIAM A. CUCHLINSKI, JR.
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 3600

Patent Examiner
MYM
Marc-Coleman Marthe

November 8, 2000